

# DS92LV090A

## 9 Channel Bus LVDS Transceiver

### General Description

The DS92LV090A is one in a series of Bus LVDS transceivers designed specifically for the high speed, low power proprietary backplane or cable interfaces. The device operates from a single 3.3V power supply and includes nine differential line drivers and nine receivers. To minimize bus loading, the driver outputs and receiver inputs are internally connected. The separate I/O of the logic side allows for loop back support. The device also features a flow through pin out which allows easy PCB routing for short stubs between its pins and the connector.

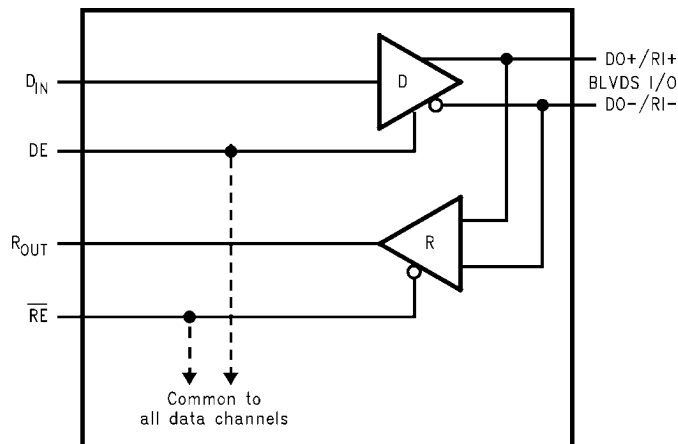
The driver translates 3V TTL levels (single-ended) to differential Bus LVDS (BLVDS) output levels. This allows for high speed operation, while consuming minimal power with reduced EMI. In addition, the differential signaling provides common mode noise rejection of  $\pm 1V$ .

The receiver threshold is less than  $\pm 100$  mV over a  $\pm 1V$  common mode range and translates the differential Bus LVDS to standard (TTL/CMOS) levels. (See Applications Information Section for more details.)

### Features

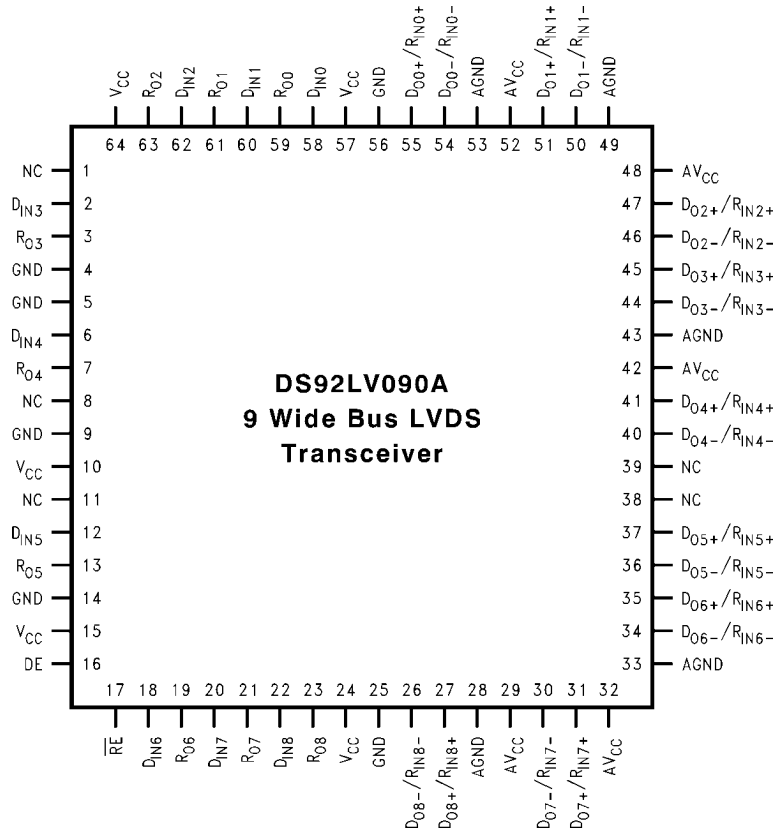
- Bus LVDS Signaling
- 3.2 nanosecond propagation delay max
- Chip to Chip skew  $\pm 800$ ps
- Low power CMOS design
- High Signaling Rate Capability (above 100 Mbps)
- 0.1V to 2.3V Common Mode Range for  $V_{ID} = 200$ mV
- $\pm 100$  mV Receiver Sensitivity
- Supports open and terminated failsafe on port pins
- 3.3V operation
- Glitch free power up/down (Driver & Receiver disabled)
- Light Bus Loading (5 pF typical) per Bus LVDS load
- Designed for Double Termination Applications
- Balanced Output Impedance
- Product offered in 64 pin TQFP package
- High impedance Bus pins on power off ( $V_{CC} = 0V$ )
- Driver Channel to Channel skew (same device) 230ps typical
- Receiver Channel to Channel skew (same device) 370ps typical

### Simplified Functional Diagram



1001101

# Connection Diagram



**Top View**  
**Order Number DS92LV090ATVEH**  
**See NS Package Number VEH064DB**

10011102

## Pin Descriptions

| Pin Name         | Pin #                              | Input/Output | Descriptions  |
|------------------|------------------------------------|--------------|---|
| DO+/RI+          | 27, 31, 35, 37, 41, 45, 47, 51, 55 | I/O          | True Bus LVDS Driver Outputs and Receiver Inputs.   |
| DO-/RI-          | 26, 30, 34, 36, 40, 44, 46, 50, 54 | I/O          | Complimentary Bus LVDS Driver Outputs and Receiver Inputs.  |
| D <sub>IN</sub>  | 2, 6, 12, 18, 20, 22, 58, 60, 62   | I            | TTL Driver Input.   |
| RO               | 3, 7, 13, 19, 21, 23, 59, 61, 63   | O            | TTL Receiver Output.  |
| RE               | 17                                 | I            | Receiver Enable TTL Input (Active Low).   |
| DE               | 16                                 | I            | Driver Enable TTL Input (Active High).  |
| GND              | 4, 5, 9, 14, 25, 56                | Power        | Ground for digital circuitry (must connect to GND on PC board). These pins connected internally.                      |
| V <sub>CC</sub>  | 10, 15, 24, 57, 64                 | Power        | V <sub>CC</sub> for digital circuitry (must connect to V <sub>CC</sub> on PC board). These pins connected internally. |
| AGND             | 28, 33, 43, 49, 53                 | Power        | Ground for analog circuitry (must connect to GND on PC board). These pins connected internally.                       |
| AV <sub>CC</sub> | 29, 32, 42, 48, 52                 | Power        | Analog V <sub>CC</sub> (must connect to V <sub>CC</sub> on PC board). These pins connected internally.                |
| NC               | 1, 8, 11, 38, 39                   | N/A          | Leave open circuit, do not connect.   |

**Absolute Maximum Ratings** (Notes 1, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

|  |                              |
|--|------------------------------|
| Supply Voltage ( $V_{CC}$ )                    | 4.0V                         |
| Enable Input Voltage<br>(DE, $\overline{RE}$ ) | -0.3V to ( $V_{CC} + 0.3V$ ) |
| Driver Input Voltage ( $D_{IN}$ )              | -0.3V to ( $V_{CC} + 0.3V$ ) |
| Receiver Output Voltage<br>( $R_{OUT}$ )       | -0.3V to ( $V_{CC} + 0.3V$ ) |
| Bus Pin Voltage (DO/RI $\pm$ )                 | -0.3V to +3.9V               |
| ESD (HBM 1.5 k $\Omega$ , 100 pF)              | >4.5 kV                      |
| Driver Short Circuit Duration                  | momentary                    |
| Receiver Short Circuit Duration                | momentary                    |
| Maximum Package Power Dissipation at 25°C      |                              |
| TQFP   | 1.74 W                       |
| Derate TQFP Package                            | 13.9 mW/°C                   |
| $\theta_{ja}$                                  | 71.7°C/W                     |

|   |                 |
|---|-----------------|
| $\theta_{jc}$                           | 10.9°C/W        |
| Junction Temperature                    | +150°C          |
| Storage Temperature Range               | -65°C to +150°C |
| Lead Temperature<br>(Soldering, 4 sec.) | 260°C           |

**Recommended Operating Conditions**

|   | Min | Max | Units               |
|---|-----|-----|---------------------|
| Supply Voltage ( $V_{CC}$ )                     | 3.0 | 3.6 | V                   |
| Receiver Input Voltage                          | 0.0 | 2.4 | V                   |
| Operating Free Air Temperature                  | -40 | +85 | °C                  |
| Maximum Input Edge Rate<br>(Note 6)(20% to 80%) |     |     | $\Delta t/\Delta V$ |
| Data  |     | 1.0 | ns/V                |
| Control   |     | 3.0 | ns/V                |

**DC Electrical Characteristics**

Over recommended operating supply voltage and temperature ranges unless otherwise specified (Notes 2, 3)

| Symbol          | Parameter                                 | Conditions  | Pin                            | Min            | Typ      | Max                    | Units   |
|-----------------|---|---|--------------------------------|----------------|----------|------------------------|---------|
| $V_{OD}$        | Output Differential Voltage               | $R_L = 27\Omega$ , Figure 1                                     | DO+/RI+,<br>DO-/RI-            | 240            | 300      | 460                    | mV      |
| $\Delta V_{OD}$ | $V_{OD}$ Magnitude Change                 |   |                                |                |          | 27                     | mV      |
| $V_{OS}$        | Offset Voltage                            |   |                                | 1.1            | 1.3      | 1.5                    | V       |
| $\Delta V_{OS}$ | Offset Magnitude Change                   |   |                                |                | 5        | 10                     | mV      |
| $V_{OH}$        | Driver Output High Voltage                | $R_L = 27\Omega$  |                                |                | 1.4      | 1.65                   | V       |
| $V_{OL}$        | Driver Output Low Voltage                 | $R_L = 27\Omega$  |                                | 0.95           | 1.1      |                        | V       |
| $I_{OSD}$       | Output Short Circuit Current<br>(Note 10) | $V_{OD} = 0V$ , DE = $V_{CC}$ , Driver outputs shorted together |                                |                | 36       | 65                     | mA      |
| $V_{OH}$        | Voltage Output High (Note 11)             | $V_{ID} = +300\text{ mV}$                                       | $R_{OUT}$                      | $V_{CC} - 0.2$ |          |                        | V       |
|                 |   | Inputs Open   |                                | $V_{CC} - 0.2$ |          |                        | V       |
|                 |   | Inputs Terminated,<br>$R_L = 27\Omega$                          |                                | $V_{CC} - 0.2$ |          |                        | V       |
| $V_{OL}$        | Voltage Output Low                        | $I_{OL} = 2.0\text{ mA}$ , $V_{ID} = -300\text{ mV}$            |                                |                | 0.05     | 0.075                  | V       |
| $I_{OD}$        | Receiver Output Dynamic Current (Note 10) | $V_{ID} = 300\text{ mV}$ , $V_{OUT} = V_{CC} - 1.0V$            |                                | -110           | 75       |                        | mA      |
|                 |   | $V_{ID} = -300\text{ mV}$ , $V_{OUT} = 1.0V$                    |                                |                | 75       | 110                    | mA      |
| $V_{TH}$        | Input Threshold High                      | DE = 0V, $V_{CM} = 1.5V$  | DO+/RI+,<br>DO-/RI-            |                |          | +100                   | mV      |
| $V_{TL}$        | Input Threshold Low                       |   |                                |                | -100     |                        | mV      |
| $V_{CMR}$       | Receiver Common Mode Range                |   |                                | $ V_{ID} /2$   |          | 2.4 -  <br>$V_{ID} /2$ | V       |
| $I_{IN}$        | Input Current                             | DE = 0V, $\overline{RE} = 2.4V$ ,<br>$V_{IN} = +2.4V$ or 0V     |                                | -20            | $\pm 1$  | +20                    | $\mu A$ |
|                 |   | $V_{CC} = 0V$ , $V_{IN} = +2.4V$ or 0V                          |                                | -20            | $\pm 1$  | +20                    | $\mu A$ |
| $V_{IH}$        | Minimum Input High Voltage                |   | $D_{IN}$ , DE, $\overline{RE}$ | 2.0            |          | $V_{CC}$               | V       |
| $V_{IL}$        | Maximum Input Low Voltage                 |   |                                | GND            |          | 0.8                    | V       |
| $I_{IH}$        | Input High Current                        | $V_{IN} = V_{CC}$ or 2.4V                                       |                                | -20            | $\pm 10$ | +20                    | $\mu A$ |
| $I_{IL}$        | Input Low Current                         | $V_{IN} = GND$ or 0.4V  |                                | -20            | $\pm 10$ | +20                    | $\mu A$ |
| $V_{CL}$        | Input Diode Clamp Voltage                 | $I_{CLAMP} = -18\text{ mA}$                                     |                                | -1.5           | -0.8     |                        | V       |

| Symbol       | Parameter  | Conditions  | Pin                 | Min | Typ | Max | Units   |
|--------------|--|---|---------------------|-----|-----|-----|---------|
| $I_{CCD}$    | Power Supply Current<br>Drivers Enabled, Receivers<br>Disabled | No Load, $DE = \overline{RE} = V_{CC}$ ,<br>$DIN = V_{CC}$ or GND   | $V_{CC}$            |     | 55  | 80  | mA      |
| $I_{CCR}$    | Power Supply Current<br>Drivers Disabled, Receivers<br>Enabled | $DE = \overline{RE} = 0V$ , $V_{ID} = \pm 300mV$  |                     |     | 73  | 80  | mA      |
| $I_{CCZ}$    | Power Supply Current,<br>Drivers and Receivers TRI-<br>STATE®  | $DE = 0V$ ; $\overline{RE} = V_{CC}$ ,<br>$DIN = V_{CC}$ or GND   |                     |     | 35  | 80  | mA      |
| $I_{CC}$     | Power Supply Current,<br>Drivers and Receivers<br>Enabled      | $DE = V_{CC}$ ; $\overline{RE} = 0V$ ,<br>$DIN = V_{CC}$ or GND,<br>$R_L = 27\Omega$                          |                     |     | 170 | 210 | mA      |
| $I_{OFF}$    | Power Off Leakage Current                                      | $V_{CC} = 0V$ or OPEN,<br>$D_{IN}$ , $DE$ , $\overline{RE} = 0V$ or OPEN,<br>$V_{APPLIED} = 3.6V$ (Port Pins) | DO+/RI+,<br>DO-/RI- | -20 |     | +20 | $\mu A$ |
| $C_{OUTPUT}$ | Capacitance @ Bus Pins   |   | DO+/RI+,<br>DO-/RI- |     | 5   |     | pF      |
| $C_{OUTPUT}$ | Capacitance @ $R_{OUT}$  |   | $R_{OUT}$           |     | 7   |     | pF      |

## AC Electrical Characteristics

Over recommended operating supply voltage and temperature ranges unless otherwise specified (Note 6)

| Symbol   | Parameter  | Conditions   | Min   | Typ  | Max  | Units |    |
|--|--|--|---|------|------|-------|----|
| <b>DIFFERENTIAL DRIVER TIMING REQUIREMENTS</b>   |  |  |   |      |      |       |    |
| $t_{PHLD}$                                       | Differential Prop. Delay High to Low (Note 8)      | $R_L = 27\Omega$ ,<br>Figures 2, 3,<br>$C_L = 10\text{ pF}$  | 0.6   | 1.4  | 2.2  | ns    |    |
| $t_{PLHD}$                                       | Differential Prop. Delay Low to High (Note 8)      |  | 0.6   | 1.4  | 2.2  | ns    |    |
| $t_{SKD1}$                                       | Differential Skew $ t_{PHLD} - t_{PLHD} $ (Note 9) |  |   | 80   |      | ps    |    |
| $t_{SKD2}$                                       | Chip to Chip Skew (Note 12)                        |  |   |      | 1.6  | ns    |    |
| $t_{SKD3}$                                       | Channel to Channel Skew (Note 13)                  |  |   | 0.25 | 0.45 | ns    |    |
| $t_{TLH}$  | Transition Time Low to High                        |  |   |      | 0.6  | 1.2   | ns |
| $t_{THL}$  | Transition Time High to Low                        |  |   |      | 0.5  | 1.2   | ns |
| $t_{PHZ}$  | Disable Time High to Z                             |  | $R_L = 27\Omega$ ,<br>Figures 4, 5,<br>$C_L = 10\text{ pF}$ |      | 3    | 8     | ns |
| $t_{PLZ}$  | Disable Time Low to Z                              |  |   | 3    | 8    | ns    |    |
| $t_{PZH}$  | Enable Time Z to High                              |  |   | 3    | 8    | ns    |    |
| $t_{PZL}$  | Enable Time Z to Low                               |  |   | 3    | 8    | ns    |    |
| <b>DIFFERENTIAL RECEIVER TIMING REQUIREMENTS</b> |  |  |   |      |      |       |    |
| $t_{PHLD}$                                       | Differential Prop. Delay High to Low (Note 8)      | $R_L = 50\Omega$ ,<br>Figures 6, 7,<br>$C_L = 35\text{ pF}$  | 1.6   | 2.4  | 3.2  | ns    |    |
| $t_{PLHD}$                                       | Differential Prop Delay Low to High (Note 8)       |  | 1.6   | 2.4  | 3.2  | ns    |    |
| $t_{SDK1}$                                       | Differential Skew $ t_{PHLD} - t_{PLHD} $ (Note 9) |  |   | 80   |      | ps    |    |
| $t_{SDK2}$                                       | Chip to Chip Skew (Note 12)                        |  |   |      | 1.6  | ns    |    |
| $t_{SDK3}$                                       | Channel to Channel Skew (Note 13)                  |  |   | 0.35 | 0.60 | ns    |    |
| $t_{TLH}$  | Transition Time Low to High                        |  |   |      | 1.5  | 2.5   | ns |
| $t_{THL}$  | Transition Time High to Low                        |  |   | 1.5  | 2.5  | ns    |    |
| $t_{PHZ}$  | Disable Time High to Z                             | $R_L = 500\Omega$ ,<br>Figures 8, 9,<br>$C_L = 35\text{ pF}$ |   | 4.5  | 10   | ns    |    |
| $t_{PLZ}$  | Disable Time Low to Z                              |  |   | 3.5  | 8    | ns    |    |
| $t_{PZH}$  | Enable Time Z to High                              |  |   | 3.5  | 8    | ns    |    |
| $t_{PZL}$  | Enable Time Z to Low                               |  |   | 3.5  | 8    | ns    |    |

**Note 1:** "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

**Note 2:** All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified except  $V_{OD}$ ,  $\Delta V_{OD}$  and  $V_{ID}$ .

**Note 3:** All typicals are given for  $V_{CC} = +3.3\text{V}$  and  $T_A = +25^\circ\text{C}$ , unless otherwise stated.

**Note 4:** ESD Rating: HBM (1.5 k $\Omega$ , 100 pF) > 4.5 kV EIAJ (0 $\Omega$ , 200 pF) > 300V.

**Note 5:**  $C_L$  includes probe and fixture capacitance.

**Note 6:** Generator waveforms for all tests unless otherwise specified:  $f = 25\text{ MHz}$ ,  $Z_O = 50\Omega$ ,  $t_r, t_f = <1.0\text{ ns}$  (0%–100%). To ensure fastest propagation delay and minimum skew, data input edge rates should be equal to or faster than 1ns/V; control signals equal to or faster than 3ns/V. In general, the faster the input edge rate, the better the AC performance.

**Note 7:** The DS92LV090A functions within datasheet specification when a resistive load is applied to the driver outputs.

**Note 8:** Propagation delays are guaranteed by design and characterization.

**Note 9:**  $t_{SKD1} |t_{PHLD} - t_{PLHD}|$  is the worse case skew between any channel and any device over recommended operation conditions.

**Note 10:** Only one output at a time should be shorted, do not exceed maximum package power dissipation capacity.

**Note 11:**  $V_{OH}$  failsafe terminated test performed with 27 $\Omega$  connected between RI+ and RI- inputs. No external voltage is applied.

**Note 12:** Chip to Chip skew is the difference in differential propagation delay between any channels of any devices, either edge.

**Note 13:** Channel to Channel skew is the difference in driver output or receiver output propagation delay between any channels within a device, either edge.

## Applications Information

General application guidelines and hints may be found in the following application notes: AN-808, AN-903, AN-971, AN-977, and AN-1108.

There are a few common practices which should be implied when designing PCB for Bus LVDS signaling. Recommended practices are:

- Use at least 4 PCB board layer (Bus LVDS signals, ground, power and TTL signals).
  - Keep drivers and receivers as close to the (Bus LVDS port side) connector as possible.
  - Bypass each Bus LVDS device and also use distributed bulk capacitance between power planes. Surface mount capacitors placed close to power and ground pins work best. Two or three high frequency, multi-layer ceramic (MLC) surface mount (0.1  $\mu$ F, 0.01  $\mu$ F, 0.001  $\mu$ F) in parallel should be used between each  $V_{CC}$  and ground. The capacitors should be as close as possible to the  $V_{CC}$  pin. Multiple vias should be used to connect  $V_{CC}$  and Ground planes to the pads of the by-pass capacitors. In addition, randomly distributed by-pass capacitors should be used.
  - Use the termination resistor which best matches the differential impedance of your transmission line.
  - Leave unused Bus LVDS receiver inputs open (floating). Limit traces on unused inputs to <0.5 inches.
  - Isolate TTL signals from Bus LVDS signals
- MEDIA (CONNECTOR or BACKPLANE) SELECTION:**
- Use controlled impedance media. The backplane and connectors should have a matched differential impedance.

## Test Circuits and Timing Waveforms

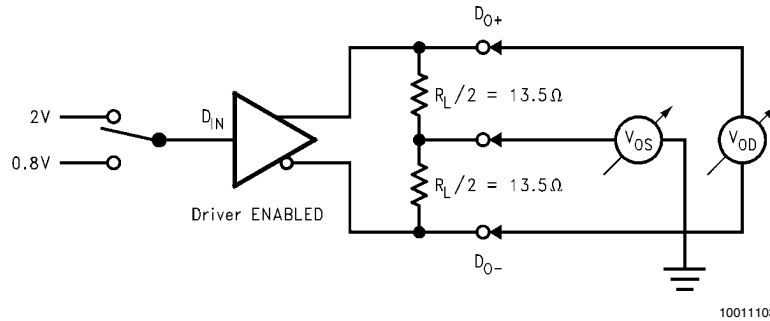


FIGURE 1. Differential Driver DC Test Circuit

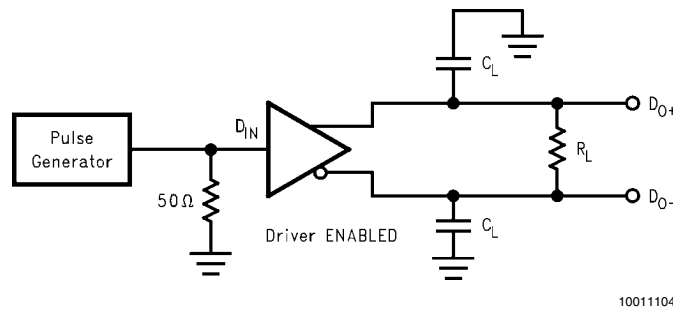


FIGURE 2. Differential Driver Propagation Delay and Transition Time Test Circuit

TABLE 1. Functional Table

| MODE SELECTED  | DE | $\overline{RE}$ |
|----------------|----|-----------------|
| DRIVER MODE    | H  | H               |
| RECEIVER MODE  | L  | L               |
| TRI-STATE MODE | L  | H               |
| LOOP BACK MODE | H  | L               |

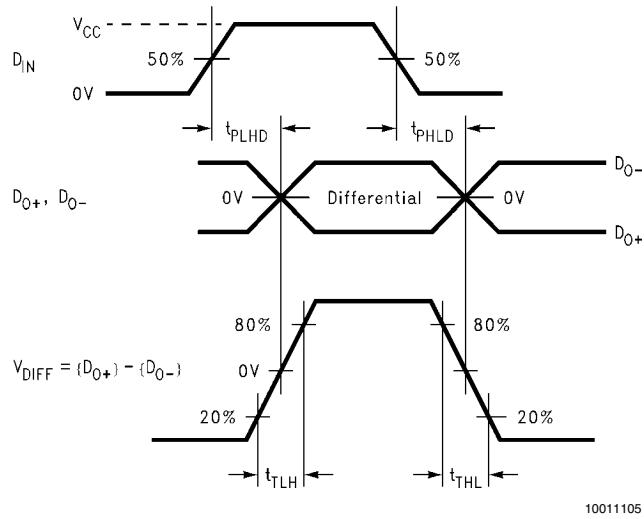
TABLE 2. Transmitter Mode

| INPUTS |                        | OUTPUTS |       |
|--------|------------------------|---------|-------|
| DE     | $D_{IN}$               | $DO+$   | $DO-$ |
| H      | L                      | L       | H     |
| H      | H                      | H       | L     |
| H      | $0.8V < D_{IN} < 2.0V$ | X       | X     |
| L      | X                      | Z       | Z     |

TABLE 3. Receiver Mode

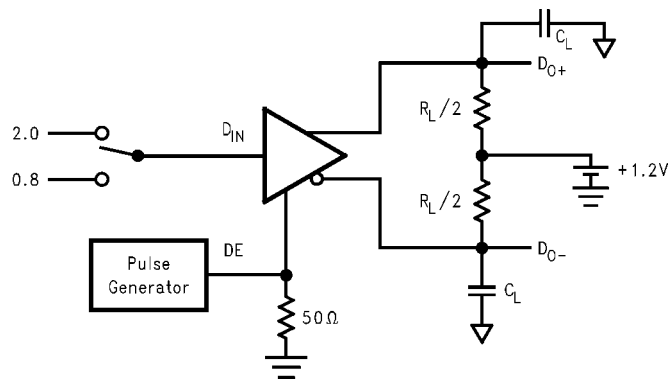
| INPUTS          |  | OUTPUT |
|-----------------|--|--------|
| $\overline{RE}$ | (RI+) – (RI-)                              |        |
| L               | L (< -100 mV)                              | L      |
| L               | H (> +100 mV)                              | H      |
| L               | $-100\text{ mV} < V_{ID} < +100\text{ mV}$ | X      |
| H               | X  | Z      |

X = High or Low logic state  
 L = Low state  
 Z = High impedance state  
 H = High state



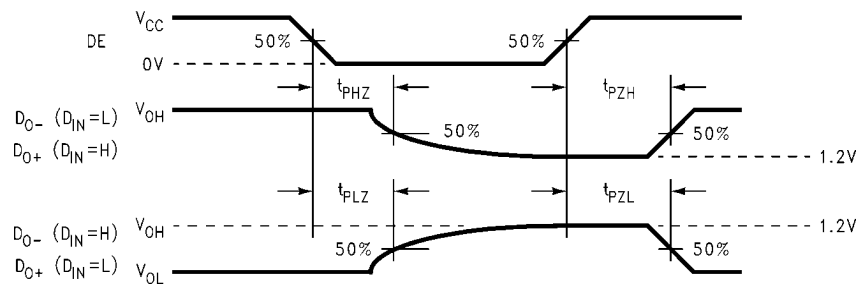
10011105

FIGURE 3. Differential Driver Propagation Delay and Transition Time Waveforms



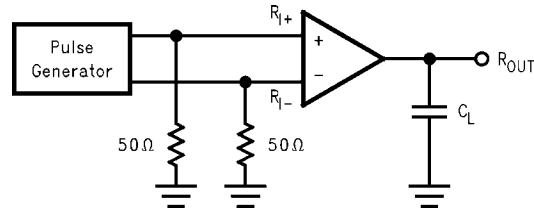
10011106

FIGURE 4. Driver TRI-STATE Delay Test Circuit



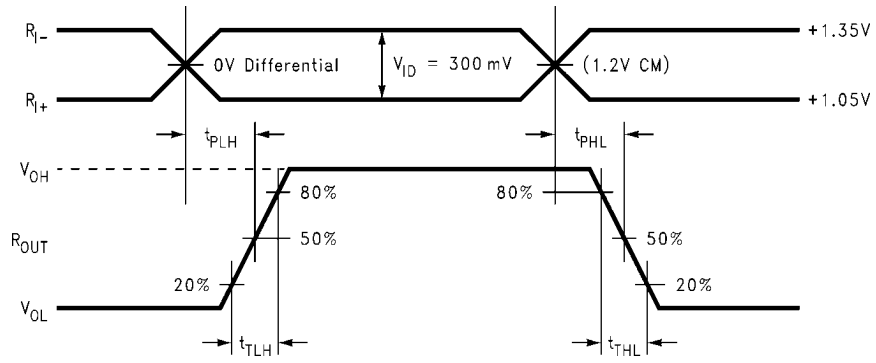
10011107

FIGURE 5. Driver TRI-STATE Delay Waveforms



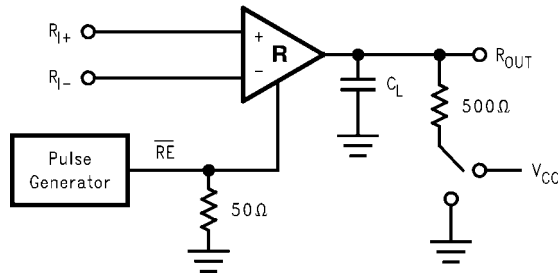
10011108

FIGURE 6. Receiver Propagation Delay and Transition Time Test Circuit



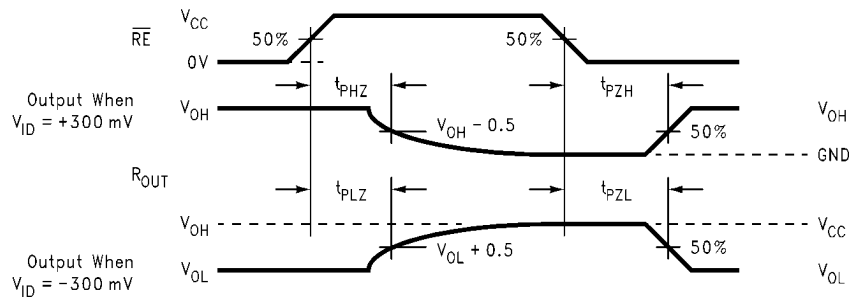
10011109

FIGURE 7. Receiver Propagation Delay and Transition Time Waveforms



10011110

FIGURE 8. Receiver TRI-STATE Delay Test Circuit

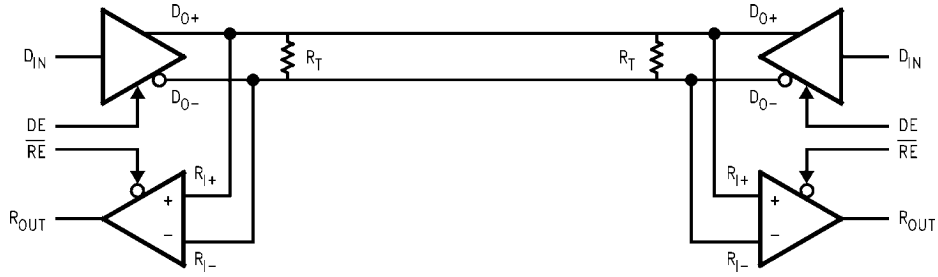


10011111

FIGURE 9. Receiver TRI-STATE Delay Waveforms

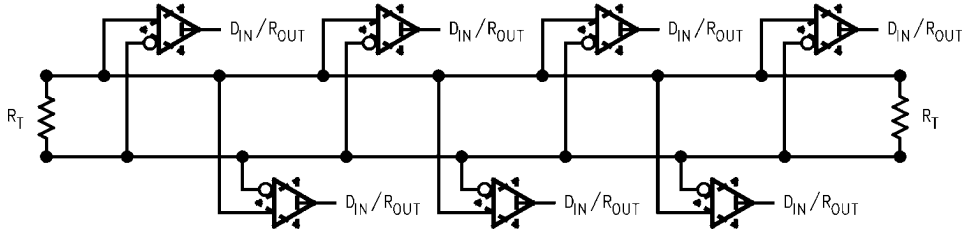


# Typical Bus Application Configurations



**Bi-Directional Half-Duplex Point-to-Point Applications**

10011112



**Multi-Point Bus Applications**

10011113



# Notes

DS92LV090A

## Notes

For more National Semiconductor product information and proven design tools, visit the following Web sites at:

| Products                       |  | Design Support          |  |
|--------------------------------|--|-------------------------|--|
| Amplifiers                     | <a href="http://www.national.com/amplifiers">www.national.com/amplifiers</a>   | WEBENCH                 | <a href="http://www.national.com/webench">www.national.com/webench</a>             |
| Audio                          | <a href="http://www.national.com/audio">www.national.com/audio</a>             | Analog University       | <a href="http://www.national.com/AU">www.national.com/AU</a>                       |
| Clock Conditioners             | <a href="http://www.national.com/timing">www.national.com/timing</a>           | App Notes               | <a href="http://www.national.com/appnotes">www.national.com/appnotes</a>           |
| Data Converters                | <a href="http://www.national.com/adc">www.national.com/adc</a>                 | Distributors            | <a href="http://www.national.com/contacts">www.national.com/contacts</a>           |
| Displays                       | <a href="http://www.national.com/displays">www.national.com/displays</a>       | Green Compliance        | <a href="http://www.national.com/quality/green">www.national.com/quality/green</a> |
| Ethernet                       | <a href="http://www.national.com/ethernet">www.national.com/ethernet</a>       | Packaging               | <a href="http://www.national.com/packaging">www.national.com/packaging</a>         |
| Interface                      | <a href="http://www.national.com/interface">www.national.com/interface</a>     | Quality and Reliability | <a href="http://www.national.com/quality">www.national.com/quality</a>             |
| LVDS                           | <a href="http://www.national.com/lvds">www.national.com/lvds</a>               | Reference Designs       | <a href="http://www.national.com/refdesigns">www.national.com/refdesigns</a>       |
| Power Management               | <a href="http://www.national.com/power">www.national.com/power</a>             | Feedback                | <a href="http://www.national.com/feedback">www.national.com/feedback</a>           |
| Switching Regulators           | <a href="http://www.national.com/switchers">www.national.com/switchers</a>     |                         |  |
| LDOs                           | <a href="http://www.national.com/ldo">www.national.com/ldo</a>                 |                         |  |
| LED Lighting                   | <a href="http://www.national.com/led">www.national.com/led</a>                 |                         |  |
| PowerWise                      | <a href="http://www.national.com/powerwise">www.national.com/powerwise</a>     |                         |  |
| Serial Digital Interface (SDI) | <a href="http://www.national.com/sdi">www.national.com/sdi</a>                 |                         |  |
| Temperature Sensors            | <a href="http://www.national.com/tempsensors">www.national.com/tempsensors</a> |                         |  |
| Wireless (PLL/VCO)             | <a href="http://www.national.com/wireless">www.national.com/wireless</a>       |                         |  |

THE CONTENTS OF THIS DOCUMENT ARE PROVIDED IN CONNECTION WITH NATIONAL SEMICONDUCTOR CORPORATION ("NATIONAL") PRODUCTS. NATIONAL MAKES NO REPRESENTATIONS OR WARRANTIES WITH RESPECT TO THE ACCURACY OR COMPLETENESS OF THE CONTENTS OF THIS PUBLICATION AND RESERVES THE RIGHT TO MAKE CHANGES TO SPECIFICATIONS AND PRODUCT DESCRIPTIONS AT ANY TIME WITHOUT NOTICE. NO LICENSE, WHETHER EXPRESS, IMPLIED, ARISING BY ESTOPPEL OR OTHERWISE, TO ANY INTELLECTUAL PROPERTY RIGHTS IS GRANTED BY THIS DOCUMENT.

TESTING AND OTHER QUALITY CONTROLS ARE USED TO THE EXTENT NATIONAL DEEMS NECESSARY TO SUPPORT NATIONAL'S PRODUCT WARRANTY. EXCEPT WHERE MANDATED BY GOVERNMENT REQUIREMENTS, TESTING OF ALL PARAMETERS OF EACH PRODUCT IS NOT NECESSARILY PERFORMED. NATIONAL ASSUMES NO LIABILITY FOR APPLICATIONS ASSISTANCE OR BUYER PRODUCT DESIGN. BUYERS ARE RESPONSIBLE FOR THEIR PRODUCTS AND APPLICATIONS USING NATIONAL COMPONENTS. PRIOR TO USING OR DISTRIBUTING ANY PRODUCTS THAT INCLUDE NATIONAL COMPONENTS, BUYERS SHOULD PROVIDE ADEQUATE DESIGN, TESTING AND OPERATING SAFEGUARDS.

EXCEPT AS PROVIDED IN NATIONAL'S TERMS AND CONDITIONS OF SALE FOR SUCH PRODUCTS, NATIONAL ASSUMES NO LIABILITY WHATSOEVER, AND NATIONAL DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY RELATING TO THE SALE AND/OR USE OF NATIONAL PRODUCTS INCLUDING LIABILITY OR WARRANTIES RELATING TO FITNESS FOR A PARTICULAR PURPOSE, MERCHANTABILITY, OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

### LIFE SUPPORT POLICY

**NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS PRIOR WRITTEN APPROVAL OF THE CHIEF EXECUTIVE OFFICER AND GENERAL COUNSEL OF NATIONAL SEMICONDUCTOR CORPORATION.** As used herein:

Life support devices or systems are devices which (a) are intended for surgical implant into the body, or (b) support or sustain life and whose failure to perform when properly used in accordance with instructions for use provided in the labeling can be reasonably expected to result in a significant injury to the user. A critical component is any component in a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system or to affect its safety or effectiveness.

National Semiconductor and the National Semiconductor logo are registered trademarks of National Semiconductor Corporation. All other brand or product names may be trademarks or registered trademarks of their respective holders.

Copyright© 2007 National Semiconductor Corporation

For the most current product information visit us at [www.national.com](http://www.national.com)



**National Semiconductor  
Americas Customer  
Support Center**  
Email:  
[new.feedback@nsc.com](mailto:new.feedback@nsc.com)  
Tel: 1-800-272-9959

**National Semiconductor Europe  
Customer Support Center**  
Fax: +49 (0) 180-530-85-86  
Email: [europe.support@nsc.com](mailto:europe.support@nsc.com)  
Deutsch Tel: +49 (0) 69 9508 6208  
English Tel: +49 (0) 870 24 0 2171  
Français Tel: +33 (0) 1 41 91 8790

**National Semiconductor Asia  
Pacific Customer Support Center**  
Email: [ap.support@nsc.com](mailto:ap.support@nsc.com)

**National Semiconductor Japan  
Customer Support Center**  
Fax: 81-3-5639-7507  
Email: [jpn.feedback@nsc.com](mailto:jpn.feedback@nsc.com)  
Tel: 81-3-5639-7560